IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 10/615,507
Filed: July 8, 2003
Inventor:
Mitchell Alsup

Title: System and Method of Identifying Liveness Groups within Traces Stored in a Trace Cache

Examiner: Nguyen, Hiep T.
Group/Art Unit: 2187
Atty. Dkt. No: 5500-79600

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Robert C. Kowert

Oct. 3, 2005
Date

Signature

DECLARATION

1. I am the named inventor of the above-referenced application.

2. I conceived of a microprocessor including a trace cache configured to cache traces and/or at least partially decoded operations. The trace cache includes one or more trace cache entries, each of which may store a trace of instructions or operations. A stored trace includes flow control information identifying whether or not operations included in each trace depend on one or more branch operations included in that trace. Collectively, these features are referred to herein as the "Trace Cache Technology."

3. At least the following portions of United States Patent Application Publication No. 2004/0143721 A1 (the "'721 application") contain a description of the Trace Cache Technology: p. 17, para. 154, lines 1-4; p. 17, para. 155, lines 1-4; and p. 17, para. 155, lines 6-12.

4. On information and belief, the Trace Cache Technology was disclosed to the inventors of the '721 application.

5. On information and belief, the inventors of the '721 application derived their knowledge of the Trace Cache Technology from me.

6. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Mitchell Alsup Sept 28 '05

Mitchell Alsup Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 10/615,507
Filed: July 8, 2003
Inventor:
Mitchell Alsup

Title: System and Method of Identifying Liveness Groups Within Traces Stored in a Trace Cache

§

Examiner: Nguyen, Hiep T.
Group/Art Unit: 2187
Atty. Dkt. No: 5500-79600

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on the date indicated below.

Robert C. Kowert

Oct. 3, 2005
Date

Signature

DECLARATION

1. We are the inventors of United States Patent Application Publication No. 2004/0143721 A1 (the "'721 application").

2. The '721 application includes a description of a microprocessor including a trace cache configured to cache traces and/or at least partially decoded operations. The trace cache includes one or more trace cache entries, each of which may store a trace of instructions or operations. A stored trace includes flow control information identifying whether or not operations included in each trace depend on one or more branch operations included in that trace. Collectively, these features are referred to herein as the "Trace Cache Technology."

3. At least the following portions of the '721 application contain a description of the Trace Cache Technology: p. 17, para. 154, lines 1-4; p. 17, para. 155, lines 1-4; and p. 17, para. 155, lines 6-12.

4. The description of the Trace Cache Technology was derived from disclosures made to one or more of us, directly or indirectly, by Mitchell Alsup.

5. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

James K. Pickett 9/24/05

James K. Pickett Date

Benjamin Thomas Sander Date

Kevin Michael Lepak Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 10/615,507	§	Examiner: Nguyen, Hiep T.
Filed: July 8, 2003	§	Group/Art Unit: 2187
Inventor:	§	Atty. Dkt. No: 5500-79600
Mitchell Alsup	§	
	§	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on the date indicated below.
	§	Robert C. Kowert
Title: System and Method of Identifying Liveness Groups Within Traces Stored in a Trace Cache	§	Oct. 3, 2005 (Date) Signature

DECLARATION

1. We are the inventors of United States Patent Application Publication No. 2004/0143721 A1 (the "'721 application").

2. The '721 application includes a description of a microprocessor including a trace cache configured to cache traces and/or at least partially decoded operations. The trace cache includes one or more trace cache entries, each of which may store a trace of instructions or operations. A stored trace includes flow control information identifying whether or not operations included in each trace depend on one or more branch operations included in that trace. Collectively, these features are referred to herein as the "Trace Cache Technology."

3. At least the following portions of the '721 application contain a description of the Trace Cache Technology: p. 17, para. 154, lines 1-4; p. 17, para. 155, lines 1-4; and p. 17, para. 155, lines 6-12.

4. The description of the Trace Cache Technology was derived from disclosures made to one or more of us, directly or indirectly, by Mitchell Alsup.

5. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

		9-19-2005	
James K. Pickett	Date	Benjamin Thomas Sander	Date

Kevin Michael Lepak	Date

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No: 10/615,507	§	Examiner: Nguyen, Hiep T.
Filed: July 8, 2003	§	Group/Art Unit: 2187
Inventor:	§	Atty. Dkt. No: 5500-79600
Mitchell Alsup	§	
	§	I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Assistant Commissioner for Patents, Washington, DC 20231, on the date indicated below.
	§	Robert C. Kowert
Title: System and Method of Identifying Liveness Groups Within Traces Stored in a Trace Cache	§	Oct. 3, 2005 (Date) Signature

DECLARATION

1. We are the inventors of United States Patent Application Publication No. 2004/0143721 A1 (the "'721 application").

2. The '721 application includes a description of a microprocessor including a trace cache configured to cache traces and/or at least partially decoded operations. The trace cache includes one or more trace cache entries, each of which may store a trace of instructions or operations. A stored trace includes flow control information identifying whether or not operations included in each trace depend on one or more branch operations included in that trace. Collectively, these features are referred to herein as the "Trace Cache Technology."

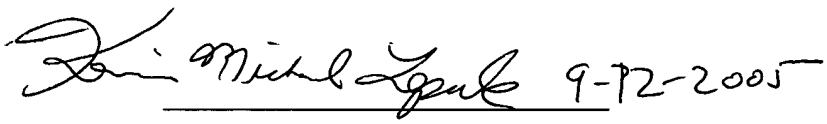
3. At least the following portions of the '721 application contain a description of the Trace Cache Technology: p. 17, para. 154, lines 1-4; p. 17, para. 155, lines 1-4; and p. 17, para. 155, lines 6-12.

4. The description of the Trace Cache Technology was derived from disclosures made to one or more of us, directly or indirectly, by Mitchell Alsup.

5. We hereby declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

James K. Pickett Date

Benjamin Thomas Sander Date



Kevin Michael Lepak Date